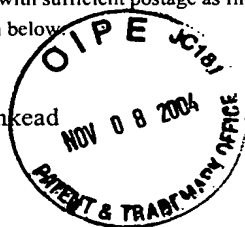


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Group Art Unit 2817
Atten: Examiner A. Kinkead
(703) 872-9306



PATENT
Docket No.: RFM-006 US

On 1 NOVEMBER 2004
By: Clifford B. Perry
Clifford B. Perry, Reg. No. 43,854

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 10/605,635
Applicants : Lazarescu et al.
Filed : Oct. 15, 2003
Art Unit : 2817
Examiner : A. Kinkead

Docket No. : RFM-006 US
Customer No. : 30499
Confirm No. : 2634

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**Preliminary Amendment and
Information Disclosure Statement**

Examiner Kinkead:

Enclosed, please find the following documents:

- (1) Preliminary Amendment of pending claims; and
- (2) An Information Disclosure Statement identifying patent and non-references.

Paper copies of non-patent references are being mailed under separate cover.

Should any questions arise, the Examiner is invited to e-mail the Applicants' representative, Clifford Perry at cperry@perryiplaw.com and indicate a day and time when a return telephone call to the Examiner would be most convenient.

Respectfully submitted,

Clifford B. Perry
Reg. No. 43,854
Attorney for Applicants

449 Santa Fe Drive, # 312
Encinitas, CA 92024
cperry@perryiplaw.com

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Preliminary Amendment

Examiner Kinhead:

Prior to examination on the merits, the Applicants request amendment to the claims as provided in pages 2-5 or this paper.

Amendments to the Claims

The listing of the claims will replace all prior version, and listings of claims in the application:

Listing of Claims:

Claim 1 (currently amended): An oscillator circuit, which comprises:

a tank circuit having a first port and a second port, the tank circuit configured to resonate at one or more predefined frequencies;

a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port; and

a gain-cell tuning inductor coupled between the third ports of the first and second oscillator transistors;

a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit; and

a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit,

wherein the gain-cell tuning inductor is operable to conduct a bias signal supplied thereto to the third ports of the first and second oscillator transistors.

Claim 2 (original): The oscillator circuit of claim 1, further comprising a supply resistor having a first port coupled to the first ports of the first and second oscillator transistors.

Claim 3 (canceled).

Claim 4 (original): The oscillator circuit of claim 1, wherein the tank circuit comprises:

first and second varactor diodes coupled in series and between the first and second ports of the tank circuit; and

a tank inductor coupled between the first and second ports of the tank circuit.

Claim 5 (original): The oscillator circuit of claim 1, wherein the tank inductor is coupled to first potential, and the first ports of first and second oscillator transistors are coupled to a second potential.

Claim 6 (original): The oscillator circuit of claim 5, wherein the first and second oscillator transistors comprise PMOS FET transistors or p-type bipolar transistors.

Claim 7 (original): The oscillator circuit of claim 6, wherein the first potential is ground potential and the second potential ranges from +2.7 to +3.6 VDC.

Claim 8 (original): The oscillator circuit of claim 5, wherein the first and second oscillator transistors comprise NMOS FET transistors or n-type bipolar transistors.

Claim 9 (original): The oscillator circuit of claim 8, wherein the first potential ranges from +2.7 to +3.6 VDC, and the second potential is ground potential.

Claim 10 (currently amended): An integrated oscillator circuit, which comprises:

- a tank circuit having a first port and a second port, the tank circuit configured to resonate at one or more predefined frequencies;

- a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

- a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port;

- a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit;

- a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit; and

- a bias supply circuit configured to generate a biasing signal, comprising:

- a bias transistor having a first port, a second port, and a third port, wherein the second and third ports are coupled together;

- a first bias circuit resistor coupled to the first port of the bias transistor;

- a second bias circuit resistor coupled to the second port of the bias transistor; and

a gain-cell tuning inductor coupled between the third ports of the first and second oscillator transistors, and coupled to the second port of the bias transistor to receive the biasing signal,

wherein the gain-cell tuning inductor is operable to conduct the bias signal to the third ports of the first and second oscillator transistors.

Claim 11 (original): The integrated oscillator circuit of claim 10, further comprising a supply resistor having a first port coupled to the first ports of the first and second oscillator transistors.

Claim 12 (canceled).

Claim 13 (original): The integrated oscillator circuit of claim 10, wherein the tank circuit comprises:

first and second varactor diodes coupled in series and between the first and second ports of the tank circuit; and

a tank inductor coupled between the first and second ports of the tank circuit.

Claim 14 (original): The oscillator circuit of claim 10, wherein the second bias circuit resistor and the tank inductor are coupled to first potential, and the first bias circuit resistor and the first ports of first and second oscillator transistors are coupled to a second potential.

Claim 15 (original): The oscillator circuit of claim 14, wherein the first and second oscillator transistors comprise PMOS FET transistors or p-type bipolar transistors.

Claim 16 (original): The oscillator circuit of claim 15, wherein the first potential is ground potential and the second potential ranges from +2.7 to +3.6 VDC.

Claim 17 (original): The oscillator circuit of claim 14, wherein the first and second oscillator transistors comprise NMOS FET transistors or n-type bipolar transistors.

Claim 18 (original): The oscillator circuit of claim 17, wherein the first potential ranges from +2.7 to +3.6 VDC, and the second potential is ground potential.

Claim 19 (currently amended): An oscillator circuit comprising:

tank circuit means for resonating at one or more predefined frequencies, the tank circuit means having a first port and a second port;

gain cell means for providing negative impedance to compensate losses in the tank circuit; the gain cell means comprising:

a first oscillator transistor having a first port, a second port coupled to the first port of the tank circuit, and a third port;

a second oscillator transistor having a first port, a second port coupled to the second port of the tank circuit, and a third port; and

gain-cell tuning means for increasing the open-loop gain of the gain cell means, the gain cell tuning means coupled between the third ports of the first and second oscillator transistors,

a first capacitor coupled between the third port of the first oscillator transistor and the second port of the tank circuit; and

a second capacitor coupled between the third port of the second oscillator transistor and the first port of the tank circuit,

wherein the gain-cell tuning means is operable to conduct the bias signal to the third ports of the first and second oscillator transistors.

Claim 20 (canceled):

REMARKS

Claim 1 has been amended to include the features of claim 3; claim 10 amended to include the features of claim 12, and claim 19 is amended to include the features of claim 20. Claims 3, 12, and 20 are now canceled without prejudice. Upon entry of the present amendment, claims 1-2, 4-11, and 13-19 are pending, the consideration of which is respectfully requested.

Conclusion

The Applicants submit that the pending claims are in condition for allowance and no outstanding issues on patentability remain. Accordingly, the issuance of a Notice of Allowance is requested.

Should any questions arise, the Examiner is invited to e-mail the Applicants' representative, Clifford Perry at cperry@perryiplaw.com and indicate a day and time when a return telephone call to the Examiner would be most convenient.

Respectfully submitted,




Clifford B. Perry
Reg. No. 43,854
Attorney for Applicants

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Information Disclosure Statement

Examiner Kinhead:

The references cited on attached forms are being provided for consideration. The title page of the non-patent references accompany this transmission, and the complete paper copies are being mailed to your attention. The listing includes those patent references cited in an International Search Report issued for the counterpart PCT patent application, a copy of which is also attached. It is respectfully requested that all cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue from this application.

No inference should be made that the information and references cited are "prior art" as defined in 35 USC §§ 102 or 103, and the Applicant reserves the right to establish that any of the cited references are not "prior art." No representation is being made that a search has been conducted, or that this statement encompasses all the possible relevant information.

The Applicant believes that no fee is required for submission of this statement, since it is being submitted prior to the first Office Action.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Cliff B. Perry", with a stylized, looping flourish at the end.

Clifford B. Perry
Attorney for Applicants
Reg. No. 43,854

449 Santa Fe Drive, #312
Encinitas, CA 92024
cperry@perryiplaw.com

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number	10/605,635
Filing Date	10/15/2003
First Named Inventor	Lazarescu
Art Unit	2817
Examiner Name	A. Kinhead
Attorney Docket Number	RFM-006 US

Sheet	1	of	1
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U. S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

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Examiner Signature		Date Considered	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number 10/605,635

Filing Date 10/15/2003

First Named Inventor Lazarescu

Art Unit 2817

Examiner Name A. Kinkead

Attorney Docket Number RFM-006 US

Sheet

1

of

1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		ZANNOTH, M. et. al, "A Single-Chip Si-Bipolar 1.6 GHz VCO with Integrated-Bias Network," IEEE Trans. MTT (NY), vol. 48, no. 2, Feb. 2000, pgs. 203-205.	
		LI, H. et al., "47 GHz VCO with Low Phase Noise Fabricated in a SiGe Bipolar Production Technology," IEEE Microw. and Wireless Cmpnt. Ltrs, vol. 12, no. 3 Mar. 2002, pgs 79-81	
		DERANTER, C. et. al. "High Data Rate Transmitter Circuits: RF CMOS Design and Tecniques for Design Automation," Kluwer Academic Publishers, ISBN 1402075456, pgs. 177-179	
		ISMAIL, A. et. al. "CMOS Differential LC Oscillator with Suppressed US-Converted Flicker Noise," IEEE Int'l Solid-State Circuits Conf., Sept. 2003.	

Examiner Signature	Date Considered
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1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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